WHAT IS CLAIMED IS

1. A capacitive high-side switch driver comprising:

an inverter having an input for receiving an input signal;

a first totem-pole buffer and a second totem-pole buffer, wherein said first totem-pole buffer is driven by said input signal and said second totem-pole buffer is driven by an output of said inverter;

a first high-voltage capacitor and a second high-voltage capacitor, wherein the outputs of said first and second totem-pole buffers drive said first and second high-voltage capacitors respectively;

a high-side transistor and a low-side transistor;

a high-side circuit having an output terminal for driving said high-side transistor, wherein said first and second high-voltage capacitors are coupled to an input of said high-side circuit;

a charge-pump diode having an anode supplied with a bias voltage;

a bootstrap capacitor connected in series with said charge-pump diode, wherein said bootstrap capacitor has a negative terminal connected to a source of said high-side transistor, wherein said bootstrap capacitor has a positive terminal connected to a cathode of said charge-pump diode; and

a bridge rectifier, wherein an input terminal of said bridge rectifier is connected to the input of said high-side circuit, wherein an output terminal of said bridge rectifier is connected in parallel with said bootstrap capacitor.

2. The capacitive high-side switch driver according to claim 1, wherein said first and second totem-pole buffers are controlled to alternately conduct in response to said input signal, wherein the duty cycles of said first and second totem-pole buffers are

complementary.

3. The capacitive high-side switch driver according to claim **1**, wherein said bias voltage will charge said bootstrap capacitor and create a floating voltage to supply power for said high-side circuit, whenever said low-side transistor is turned on.

4. The capacitive high-side switch driver according to claim **1,** wherein said first and second totem-pole buffers associate with said first and second high-voltage capacitors to generate differential signals and produce a differential voltage across said input of said high-side circuit.

5. The capacitive high-side switch driver according to claim **1**, wherein said bridge rectifier consists of four rectifiers, wherein said differential signals charge said bootstrap capacitor via said bridge-rectifier, wherein said differential signals enable said bootstrap capacitor to supply additional power to said high-side circuit.

6. The capacitive high-side switch driver according to claim **1**, wherein said high-side circuit comprises:

a comparator having a turn-on threshold, wherein an input of said comparator is connected to said input of said high-side circuit;

a drive-buffer having an output for driving a gate of said high-side transistor, wherein an input of said drive-buffer is connected to an output of said comparator;

a programmable load for providing variable impedance in response to a signal from said output of said comparator, wherein said programmable load is connected in parallel with said input of said comparator, wherein an input of said programmable load is connected to said output of said comparator;

an under-voltage protector for detecting the floating voltage of said bootstrap capacitor, wherein said under-voltage protector is connected in parallel with said

bootstrap capacitor, wherein an output of said under-voltage protector is connected to an enable terminal of said drive-buffer; and

a pull-low resistor for turning off said high-side transistor, wherein said pull-low resistor is connected from said output of said drive-buffer to said negative terminal of said bootstrap capacitor, wherein said pull-low resistor is used to turn-off said high-side transistor whenever said drive-buffer is disabled.

7. The capacitive high-side switch driver according to claim **6**, wherein said comparator will output a logic-high signal whenever the differential voltage across the input of said comparator exceeds a turn-on threshold voltage.

8. The capacitive high-side switch driver according to claim **6**, wherein said under-voltage protector enables said drive-buffer whenever the floating voltage exceeds a start threshold voltage, wherein said under-voltage protector disables said drive-buffer whenever the floating voltage drops below a stop threshold voltage.

9. The capacitive high-side switch driver according to claim **6**, wherein said programmable load has a low impedance whenever said comparator outputs a logic-low signal, wherein the impedance of said programmable load increases in proportion to the logic-high output period of said comparator.

10. The high-side circuit according to claim **6**, wherein said programmable load comprises:

a pl-vcc terminal connected to said positive terminal of said bootstrap capacitor;

a pl-ground terminal connected to said negative terminal of said bootstrap capacitor;

a pl-inverter having an input connected to said output of said comparator, wherein said input of said pl-inverter is connected to said input of said programmable load;

a pl-n transistor, wherein a gate of said pl-n transistor is connected to an output of said pl-inverter, wherein a source of said pl-n transistor is connected to said pl-ground terminal;

a constant current source connected between said pl-vcc terminal and a drain of said pl-n transistor;

a pl-capacitor connected from said drain of said pl-n transistor to said pl-ground terminal;

a first pl-buffer having a first input-threshold voltage level;

a second pl-buffer having a second input-threshold voltage level;

a third pl-buffer having a third input-threshold voltage level, wherein an input of said first pl-buffer, an input of said second pl-buffer, and an input of said third pl-buffer are connected together to said drain of said pl-n transistor;

a first pl-p transistor having a gate connected to an output of said first pl-buffer;

a first pl-resistor connected in series with said first pl-p transistor, wherein said first pl-p transistor and said first pl-resistor are connected in parallel with said input of said comparator;

a second pl-p transistor having a gate connected to an output of said second pl-buffer;

a second pl-resistor connected in series with said second pl-p transistor, wherein said second pl-p transistor and said second pl-resistor are connected in parallel with said input of said comparator;

a third pl-p transistor having a gate connected to an output of said third pl-buffer; and

a third pl-resistor connected in series with said third pl-p transistor, wherein said

third pl-p transistor and said third pl-resistor are connected in parallel with said input of said comparator.

11. The high-side circuit according to claim **10**, wherein said constant current source will start to charge said pl-capacitor so as to increase the voltage across said pl-capacitor, whenever said comparator outputs a logic-high signal.

12. The high-side circuit according to claim **10**, wherein said first pl-p transistor will be turned off as the voltage of said pl-capacitor exceeds said first input-threshold voltage level, wherein said second pl-p transistor will be turned off as the voltage of said pl-capacitor exceeds said second input-threshold voltage level, wherein said third pl-p transistor will be turned off as the voltage of said pl-capacitor exceeds said third input-threshold voltage level.

13. The high-side circuit according to claim **6**, wherein said under-voltage protector comprises:

an uv-vcc terminal connected to said positive terminal of said bootstrap capacitor;

an uv-ground terminal connected to said negative terminal of said bootstrap capacitor;

a first uv-resistor and a second uv-resistor;

a first zener diode and a second zener diode connected in series with said first uv-resistor and second uv-resistor, wherein said first zener diode is connected to said uv-vcc terminal and said second uv-resistor is connected to said uv-ground terminal;

a first uv-n transistor having a gate connected to the junction of said second zener diode and said first uv-resistor, wherein a source of said first uv-n transistor is connected to said uv-ground terminal;

an uv-p transistor having a gate connected to a drain of said first uv-n transistor,

wherein said uv-p transistor has a source and a drain connected in parallel with said first zener diode;

a third uv-resistor connected from said gate of said uv-p transistor to the uv-vcc terminal;

an uv-buffer having an input connected to said drain of said first uv-n transistor, wherein an output of said uv-buffer is connected to said enable terminal of said drive-buffer, wherein said output of said uv-buffer is further connected to an output of said under-voltage protector; and

a second uv-n transistor, wherein said output of said uv-buffer drives a gate of said second uv-n transistor, wherein a drain of said second uv-n transistor is connected to the junction of said first uv-resistor and said second uv-resistor, wherein a source of said second uv-n transistor is connected to the uv-ground terminal.